

Information Flow Tracking using an FPGA

1 Overall flow

[Flow graph]

IFT-enhanced design - IED

IFT testbench - ITB

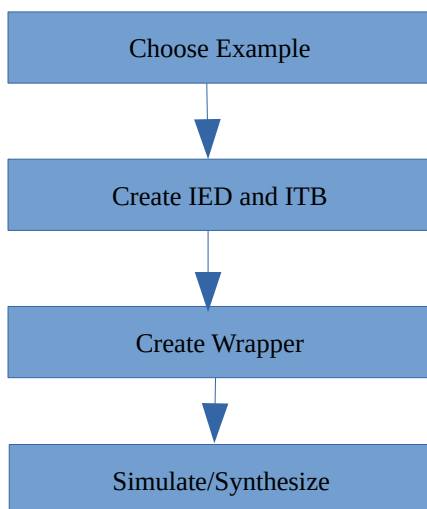
FPGA

Programmable Logic - PL

Processor - CPU

2 Steps for the implementation

1. Manual trial
 1. Choose a small example design
 2. Create IED and ITB (using DU program)
 3. Create a wrapper to implement a hard coded testbench within PL
 4. Simulate, synthesize, and run design and testbench for PL



Flow chart of the steps required

2. Architectural design

The design has usually more inputs than can directly be fed from outside the FPGA. We can use the PL for the design and the CPU for control.

 1. Develop generic architecture for tagging and simulation control of an IED
 - Stimuli data is stored in off-chip memory (DRAM) and loaded under control of the CPU.
 - Design must be able to stall
 - Tagging stimuli are created by the CPU

- CPU controls stimulation and tagging
2. Design generic wrapper and program for data exchange.
 3. Create implementation for two example designs.

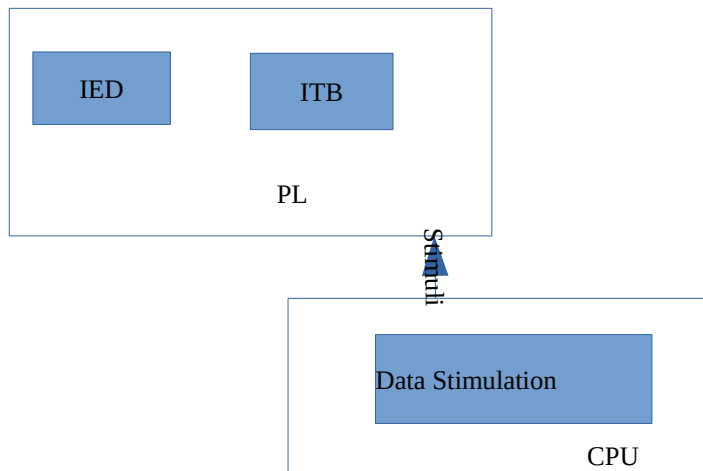


Diagram describing the System

3. Automated generation of architecture
4. Improve observability of internal tagging information of IED